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predetermined distance in the range of not less than 10% but not greater than 40% of a thickness of said insulator film.

REMARKS

Claims 32, 33, 36, 37, 41, 42, 45 and 46 have been amended to obviate the § 112 rejection. Pursuant to 37 CFR § 1.121, a marked copy of the amended claims showing the changes made therein accompanies this Amendment.

Claims 12, 16, 21, 25, 30, 34, 39 and 43 have been canceled, without prejudice, thereby rendering moot the objection under 37 CFR § 1.75.

Turning now to the rejection of claims 11-46 as obvious over Kuwajima in view of Roberts et al., McDavid, Miller et al. and Kim et al., as noted *supra*, claims 12, 16, 21, 25, 30, 34, 39 and 43 have been cancelled. As to the remaining claims, Applicant respectfully submits that this rejection has been made in error. Claims 11, 20, 29 and 38 all require that the large and small contact holes "reach said semiconductor substrate," and that the plug "contact said semiconductor substrate." On page 4, paragraph 3 of the Official Action, the Examiner cites Kuwajima as showing "that the barrier layers 13 a, b (Figure 3) and 13 (Figure 10) are part of the plug and can be allowed to remain at the bottom of the large via or not. For a plug material which does not require a barrier it would be obvious to omit the barrier." On page 5, paragraph 2 of the Official Action, the Examiner states:

Applicant states that the references do not show a plug that reaches the substrate which is apparently a reference to the barrier material being between the plug and the substrate. Note that it is known in the art to use a barrier with materials such as W but that with materials that do not need a barrier it would be obvious to omit it, as noted above.

HAYES SOLOWAY P.C.
130 W. CUSHING ST.
TUCSON, AZ 85701
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

The Examiner states that Applicant is referring to "the barrier material being between the plug and the substrate." However, this is not what Applicant is referring to; it is the well layer 2 of Kuwajima, not barrier material, that is disposed between the plug and the substrate in Kuwajima, and it is the well layer that the contact holes in Kuwajima reach, not the substrate.

Further, the Examiner is apparently refusing to acknowledge that Kuwajima fails to teach large and small contact holes that reach the semiconductor substrate and a small contact hole whose plug contacts the semiconductor substrate. To the contrary, as shown in Kuwajima Figures 10 and 11, the holes do not reach the semiconductor substrate, nor does the plug contact the semiconductor substrate (the semiconductor substrate is not shown in Figures 10 and 11). As set forth in Kuwajima at column 7, lines 50-53, it is explained that Figures 1-6 and the corresponding description apply to the embodiments illustrated in Figures 10 and 11. As can be seen from Figures 1 and 2, there is a well layer 2 above the substrate 1, and holes 15 a and 15 c, as well as the insulating film 12, all contact the well layer 2, not the substrate 1. In fact, none of the references cited by the Examiner, including Roberts et al., McDavid, Miller et al. and Kim et al. teaches large and small contact holes that reach the semiconductor substrate and a small contact hole whose plugs contact the semiconductor substrate. Further, neither Roberts et al., McDavid, Miller et al. nor Kim et al. teaches large and small contact holes, as has been argued extensively in the earlier prosecution and in two previous Appeal Briefs, which are incorporated herein by reference. Because Kuwajima, in combination with Roberts et al., McDavid, Miller et al. and Kim et al. does not teach this aspect of claims 11, 20, 29 and 38, it cannot be said that these claims are obvious over the references cited, and the same is true for all claims dependent therefrom.

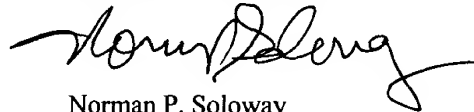
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175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

Having dealt with all the objections raised by the Examiner, the Application is believed to be in order for allowance. Early and favorable Action are respectfully requested.

In the event there are any fee deficiencies or additional fees are payable, please charge them (or credit any overpayment) to our deposit account number 08-1391.

Respectfully submitted,



Norman P. Soloway
Attorney for Applicant
Registration No. 24,315

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner of Patents and Trademarks, Washington, D.C. 20231 on April 9, 2003 at Tucson, Arizona.

By Kim Good

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HAYES SOLOWAY P.C.
130 W. CUSHING ST.
TUCSON, AZ 85701
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567



MARKED CLAIMS SHOWING CHANGES MADE

32. (Amended) A semiconductor device claimed in Claim 31, wherein said refractory conductive material covers a sidewall surface of said large diameter contact hole to a predetermined distance [is] in the range of not less than 10% but not greater than 40% of a thickness of said insulator film.

33. (Amended) A semiconductor device claimed in Claim 29, wherein said refractory conductive material covers a sidewall surface of said large diameter contact hole to a predetermined distance [is] in the range of not less than 10% but not greater than 40% of a thickness of said insulator film.

36. (Amended) A semiconductor device claimed in Claim 35, wherein said refractory conductive material covers a sidewall surface of said large diameter contact hole to a predetermined distance [is] in the range of not less than 10% but not greater than 40% of a thickness of said insulator film.

37. (Amended) A semiconductor device claimed in Claim 34, wherein said refractory conductive material covers a sidewall surface of said large diameter contact hole to a predetermined distance [is] in the range of not less than 10% but not greater than 40% of a thickness of said insulator film.

41. (Amended) A semiconductor device claimed in Claim 40, wherein said refractory conductive material covers a sidewall surface of said large diameter contact hole to a predetermined distance [is] in the range of not less than 10% but not greater than 40% of a thickness of said insulator film.

42. (Amended) A semiconductor device claimed in Claim 38, wherein said refractory conductive material covers a sidewall surface of said large diameter contact hole to a predetermined distance [is] in the range of not less than 10% but not greater than 40% of a thickness of said insulator film.

45. (Amended) A semiconductor device claimed in Claim 44, wherein said refractory conductive material covers a sidewall surface of said large diameter contact hole to a predetermined distance [is] in the range of not less than 10% but not greater than 40% of a thickness of said insulator film.

46. (Amended) A semiconductor device claimed in Claim 43, wherein said refractory conductive material covers a sidewall surface of said large diameter contact hole to a predetermined distance [is] in the range of not less than 10% but not greater than 40% of a thickness of said insulator film.